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Specifications and Interfaces

Crimson TNG is a wide band, high gain, direct conversion quadrature transceiver[1] and signal processing platform. Using analogue and digital conversion, it is capable of processing signal bandwidths up to 325MHz from approximately DC to 6.8GHz. Crimson TNG is compatible with GNU Radio and includes source code for many of its drivers and peripherals.

Absolute Maximum Ratings

Stresses beyond those listed in the Absolute Ratings Table (Table 1.1) may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and is, therefore, not recommended.

Table 1.1: Absolute Ratings: Exposure or sustained operation at absolute ratings may permanently damage Crimson TNG. Ensure fan intake vents (located on both sides of the device) are not blocked during operation.

Specifications	Min	Max	Units	Notes
Operating Temperature	5	40	C	At fan inlet
Operating Humidity	5	100	%	Non-Condensing
Storage Temperature	0	40	C	
Storage Humidity	20	95	%	Non-Condensing
Input RF Power		10	dBm	
SMA Torque	0.6	0.7	Nm	

[1] As Crimson TNG is capable of Digital Down/Up Conversion, superhet architectures can be implemented using Digital Down/Up Conversion on the FPGA.

Observed Performance

Crimson TNG is a very flexible radio and signal processing platform that supports high bandwith communications over a wide tuning range. The hardware and signal processing capabilities may be configured to support a very wide variety of applications, each with their own figures of merit. It is, therefore, fairly challenging to provide uniform performance specifications across those different configurations.

To provide a general idea of what this product is capable of, Table 1.2 on the next page lists some conservative figures of its out-of-box performance. Configuration of the product towards a specific application may see some of these figures exceed at the expense of others. For more information, please do not hesitate to contact us at: *solutions@pervices.com*.

Table 1.2: Observed Performance. These specifications reference observations taken during internal use and development. Calibration Measurements relative to 20 ° C

	Specification		Min	Nom	Max	Units
Common Radio	RF Stage (ADF4355)		110		6800	MHz
	Baseband Stage		0.1		140	MHz
	Dyn. Range		25		70	dB
	SFDR				65	dB
Receive Radio	RF Input Power			-40		dBm
	Noise Figure, Rx RF St		3.1		7	dB
	Power Gain	Low	15		45	dB
		High	-10		65	dB
	Group Delay (Radio Chain)	Low		13.7		ns
		High		20		ns
ADC (Receive Converter)	Independent Channels			4		-
	ADC resolution			16		bits
	ADC Sample Rate			322.265625	325	MSPS
	Rx Sampling Bandwidth			322.265625		MHz
	Latency (input to serial)			50		ns
Receive DSP and FPGA Specifications (Default firmware)	Decimation ($\frac{f_s}{n}$)		1		256	-
	Latency (FPGA DSP)		50	500	750	ns
Transmit Radio	Transmit Power	Low	-30		18	dBm
		High	-10		15	dBm
	Group Delay (radio chain)	Low		5		ns
		High		11		ns
DAC (Transmit Converter)	Tx Output Bandwidth			322.265625		MHz
	DAC resolution			16		bits
	DAC Sample Rate			322.265625	325	MSPS
	Latency (serial to output)		50	655	804	ns
Transmit DSP and FPGA Specifications	Interpolation ($n \cdot f_s$)		1		256	-
	Latency (FPGA DSP)		96		160	ns
Digital	FPGA - Arria V ST SOC			5ASTMD3E3F31		-
	On Board Processor Core			ARM Cortex-A9 MP		
	LPDDR2 RAM			4		Gb
	NAND Flash (x8)			4		Gb
Networking	10GBASE-R, Full Duplex	each		8		Gbps
	Default IP, SFP+ Port A			10.10.10.2		-
	Default IP, SFP+ Port B			10.10.11.2		-
Internal Reference (10 MHz)	Frequency Calibration		-5		5	ppb

External Interfaces

Crimson TNG has a number of user accessible interfaces through which the device can connect to external sources and sinks. Management functions are carried out over a web page hosted by the Crimson TNG transceiver and accessible using the Management ethernet port on the front

face of the device. Data is sent over the 10Gbps SFP+ ports and receive and transmit antennas connect to the SMA connectors on the front of the device. Other peripherals ports provide access or the capability to improve functionality.

10/100 Management Port	This connects to a Linux system running on the Hard Processing System located on the FPGA silicon, and provides a unified interface by which to control and configure the remaining devices.
10GBASE-R SFP+	There are two SFP+ ports on the front panel of the device that use 10GBASE-R encoding to directly communicate with an optical module and interface with a ten gigabit network. These ports directly interface with the FPGA fabric and support high bandwidth, low latency communication between the ADCs and DACs.[2]
50Ω SMA	There are sixteen standard SMA headers. These are used to connect to external antennas, sinks, or sources, including:

Rx (x4)	The four independent receive channels may be connected to external sources or antennas
Tx (x4)	The four independent transmit channels may be connected to external antennas or sinks
Ext. Osc	For the most demanding applications, an external oscillator may be used to drive the LMK04828 outputs. This implies a completely external synchronization solution
Ext. PLL	A reference clock for local oscillator generation for the frequency synthesizers for receive and transmit PCBs
Ext. Sys	The system reference clock for converter devices and the FPGA; only present when a sysref command is issued
Ext. Dev	An external 322.265625MHz clock directly to the converter devices as well as the FPGA
Ext. Ref	An external 10MHz reference may be applied to this port in lieu of the default, internal, 10MHz reference
Int. Ref	Crimson TNG may be used to output a 10MHz reference clock to other systems
PPS	This port can be used to synchronise internal time keeping (note: this will be enabled in future releases)
TRIG	This port can be used as a trigger (note: this will be enabled in future releases)

USB 2.0	A USB port connects to the Linux system running on the Hard Processor System.
Micro-SD Slot	The FPGA and Hard Processor System may be rebooted or configured using an external Micro-SD card.
Industrial Mini I/O	GPIO connects to the FPGA
IEC320 C14 Power	A standard «computer» cable plugs into this connector to power the unit. The power supply accepts 120V or 240V.

[2]Please note, not all 10Gbps NICs support 10GBASE-R protocols - it is important that you ensure the card you select supports communication using 10GBASE-R. If you have questions about this, please do not hesitate to contact us.